REMARKS

The Applicant respectfully requests the Examiner to enter the presented amendments prior to the examination of the application. Claims 4 and 8-12 have been cancelled without prejudice. Claims 1 and 13 have been amended. Claims 1-2, 5-7, and 13-17 remain in the application. Consideration of the application as preliminarily amended is respectfully requested.

35 U.S.C. § 102(b) Rejections

In the prior final office action dated February 26, 2003 responsive to patent application number 09/457,932, the Examiner rejected claims 1-2 under 35 U.S.C. § 102(b) as being anticipated by Partovi et al. U.S. Patent 5,353, 424 (hereinafter "Partovi," et al.). Applicant will consider the 102(b) rejections in view of the amended claims in the present continuation.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Independent claim 1 of the present application includes limitations that are not disclosed or suggested by Partovi. In particular, the claim includes the limitation, or limitation similar thereto, of a multi-hit detection circuit coupled to the hit lines to detect multiple hits in the cache during the clock cycle based on hit signals on the hit lines, where the multi-hit detection circuit comprises a NAND gate with transistor pairs. Claim 1 further includes an error flag generated by an inverter output during the clock cycle in the multi-hit detection circuit. Partovi does not teach such limitations. Rather, Partovi specifically discloses the use of an XOR circuit as a means for comparing signals and producing a signal. Partovi fails to describe an error flag generated by an

inverter output. Moreover, Partovi fails to mention any use of a NAND gate in order to detect multiple hits in the cache. Rather, Partovi discloses a circuit, which couples the outputs of the XOR gates to NOR gates in order to generate a bank-select output. Therefore, Partovi does not disclose or suggest a multi-hit detection circuit comprising a NAND gate with transistor pairs or an inverter output which generates an error flag. Accordingly, Partovi does not anticipate claims 1 and 13.

Claim 2 depends from independent claim 1. Therefore, claim 2 includes the novel limitations discussed above and is patentably distinct from Partovi.

Claims 3 and 5-7 depend from independent claim 1. Therefore, the claims 3 and 5-7 include the novel claim limitations discussed above and are not anticipated by Partovi.

35 U.S.C. § 103(a) Rejections

In the prior final office action dated February 26, 2003 responsive to patent application number 09/457,932, the Examiner rejected claim 13 under 35 U.S.C. § 103(a) as being anticipated by "Fail-Soft Circuit Design in a Cache Memory Control LSI," February 1987, ISSCC 87, pp. 103-104 (hereinafter "Ooi," et al.) in view of Partovi. Examiner rejected claims 5, 6, and 15-17 under 35 U.S.C. § 103(a) as being unpatentable over Ooi in view of Partovi and Katz. Amended claims 1 and 13 include similar limitations to claims 5, 6, and 15-17, and therefore, Applicant will consider the Examiner's previous rejection in view of the amended claims in the present continuation.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Independent claims 1 and 13 have been amended to include the limitation, or limitation similar thereto, of using a NAND gate with transistor pairs to determine if any two hit signals both indicate a hit. Claims 1 and 13 further include an error flag generated by an inverter output during the clock cycle indicating the validity of the selected data.

Ooi does not teach these limitations, and therefore, the independent claims are patentable over Ooi in view of Partovi and Katz. As noted by Examiner, Ooi does not disclose the output of an error flag (Ooi, Fig. 4). Ooi does not disclose the use of a NAND gate with transistor pairs or the use of an inverter output to generate the error flag. As discussed above, Partovi does not disclose the use of a NAND gate using transistor pairs or the use of the inverter output to generate an error flag. Rather, Partovi discloses the use of an XOR circuit as a means for comparing signals. Katz describes the NAND gate in definitional terms, but fails to describe NAND gates with transistor pairs to detect multiple hit lines. Further, Katz fails to describe the use of an inverter output to generate an error flag. As such, the references fail to teach each element of claims 1 and 13.

Moreover, there is no suggestion or motivation which would lead one of ordinary skill in the art to modify Partovi to include the claimed limitations. Examiner suggests it would have been obvious to substitute a NAND gate for the logic used in the comparator of Partovi. Applicant respectfully disagrees. A person of ordinary skill in the art would not have been motivated to make this modification because the resulting combinational logic would not have achieved the desired results. In Partovi, the XOR gate yields the same signal, a cache miss, for a multi-hit error as for the condition where no hits have occurred. In the condition where two hit signals both indicate a hit, the XOR gate yields 0. Likewise, in the condition where two hit signals both indicate a miss, the XOR

gate also yields 0. In other words, an XOR circuit as used in Partovi, does not distinguish between the situations where there are multi-hits and situations where no hits have occurred. Partovi seeks to signal a cache miss when both banks miss and when both banks hit. In both conditions, Partovi recognizes that neither data item should be used, so a miss is signaled. (Partovi, column 3, lines 4 - 8).

However, substituting the NAND gate for the XOR gate in Partovi would not yield the desired results. The NAND gate distinguishes between situations where there are multi-hits and situations where no hits have occurred. Accordingly, in the case where both banks miss, the NAND gate would erroneously signal a cache hit. Additionally, in order to modify Partovi to include the limitations stated above, the modification would require four NAND gates to implement the XOR logic for a comparison of two signals. Whereas independent claims 1 and 13 disclose a NAND gate with transistor pairs. Thus there is no suggestion or motivation to modify Partovi to include the limitations of claims 1 and 13.

Furthermore, there is no suggestion or motivation which would lead one skilled in the art to modify Partovi to include the claimed limitations. Partovi fails to disclose the use of an inverter output to generate an error flag during the clock cycle. Rather, Partovi discloses the use of an inverter output as an input to a NAND gate. It would not have been obvious to one skilled in the art to switch the inverter to the output of the NAND because the inverters are required for the bank-select logic implemented. (Partovi, column 11, lines 36 – 40). Additionally, switching the placement of the inverter would fail to produce an inverter output that generates an error flag. Rather, if switched to the output of the NAND, the output of the inverter generates a bank selection. (Partovi, column 11, lines 36 –

40). Thus there is no suggestion or motivation to modify Partovi to include the limitations of claims 1 and 13.

Since Ooi, Partovi, and Katz, in combination, fail to teach each element of the above limitations and there is no motivation to modify Partovi to include such limitations, the references cannot render claims 1 and 13 obvious. Accordingly, Applicant respectfully submits that independent claims 1 and 13 are in condition for allowance.

The remaining claims depend from one of the foregoing independent claims discussed above and thus include the novel claim limitations discussed above. Therefore, the remaining claims are not anticipated by Partovi and are patentable over Ooi, Partovi, and Katz.

CONCLUSION

Applicant respectfully submits the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John P. Ward at (408) 720-8300, x237.

If there are any additional charges, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

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